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Analysis of CMOs Dynamic Comparators for Low Power and High Speed ADCs

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***Abstract*—The need for extreme low power, efficient area and high speed ADC converters make use of the dynamic comparators for maximizing the speed and efficiency of power. Generally comparators play a vital role in the ADCs circuits for comparing the input voltage with respect to the reference voltage. The comparison of the voltage with acceptable delay and operating in low voltage is a major challenge in the comparator design. Several comparators having different characteristics exist. The conventional dynamic comparators have advantages like high input impedance, no static power dissipation and good robustness against noise and mismatch. The drawback is that large numbers of transistors are used to minimize the offset, so the speed of the comparator is reduced and has the delay of 940ps/dec. Double tail comparators overcome the drawbacks in conventional comparator. There is a less stacking of transistors used with low voltage supply and delay is considerably reduced (358 ps/dec). But the trans-conductance will be low for this comparator. In low power double tail comparator, without complicating the design and by adding few transistors the positive feedback during the regeneration is strengthened with results in reduce delay time (294 ps/dec).Here several comparators are analysed and their delay will be calculated to prove why dynamic comparators will be chosen for high speed applications in analog-to-digital converters. In our proposed system the transistor technology, architecture will be modified aiming to reduce the power supply voltage, propagation delay and stacking of transistors thereby increasing the speed in ADCs circuits. In this paper, performances of various types of latched comparators are compared in terms of their delay, speed and power. The accuracy of comparators, which is defined by its delay, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. The Tool used in this paper is HSPICE.**

***Keywords*— conventional dynamic comparator, mismatch, offset, double-tail comparator, ADC-analog-to-digital converters**

1. INTRODUCTION

COMPARATOR is one of the main fundamental blocks in analog-to-digital converters. Since they are decision-making circuits that interface the analog and digital signals, the accuracy, which is often determined by its input-referred offset voltage, is essential for the resolution of high-performance ADCs. Dynamic comparators are widely used in high-speed ADCs due to its low power consumption and fast speed. Generally they use positive feedback mechanism with two pair of back-to-back cross coupled inverter to convert a small input-voltage difference to a full-scale digital level in a very short time. However, an input-referred latch offset voltage, resulting from static mismatches such as threshold voltage Vth and ß variations [2] in the regenerative latch, reduces the accuracy of such comparators. Moreover, dynamic mismatch from the unbalanced parasitic capacitances [2] on the output nodes of the latch causes the additional offset term during evaluation phase. Because of this reason, the input-referred latch offset [4] voltage is one of the most important design parameters of the latched comparator. If large numbers of devices are used for the latching stage, a low offset can be achieved. Generally the comparator called **static comparator** consists of three stages as discussed below.

A. Pre-Amplification

This stage amplifies the input signal and thus improves the comparator sensitivity. The minimum input signal increased for making the comparator to take a decision. The schematic diagram of the pre-amplification circuit is as shown below.

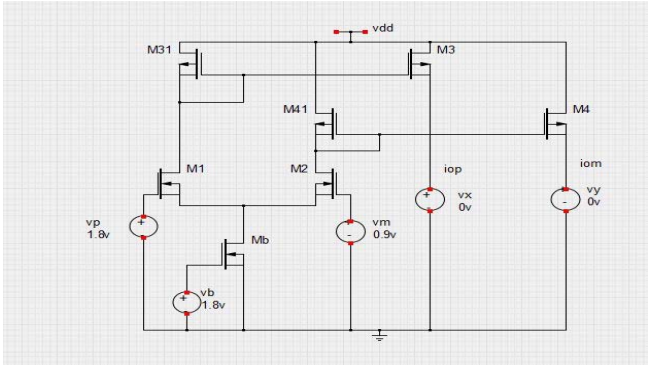

Fig-1: Pre-amplification stage

When **vp >vm** transistor M31 i.e. PMOS gets off but some small amount of current flows. As the M3 is the current mirror circuit, the same amount of current flows as in M31.In the same way, vm is small then the M41 gets on, the current flows in the transistor will be large and M4 also the same current. Therefore the current flowing through the transistor M3 is small which is denoted by **iop**. In the same way the current flowing in the M4 transistor is high denoted by **iom.** The simulation result for the current is as shown below.

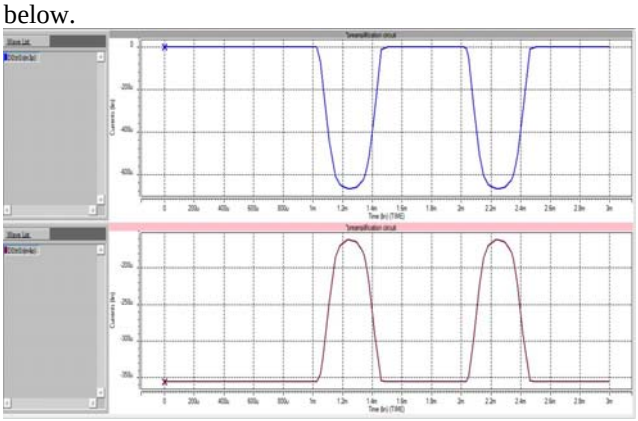

Fig-2: Simulation result

B. Decision making circuit

This stage is used to find which of the input signals is larger. This circuit uses the positive feedback. The schematic diagram of the decision circuit is as shown below.

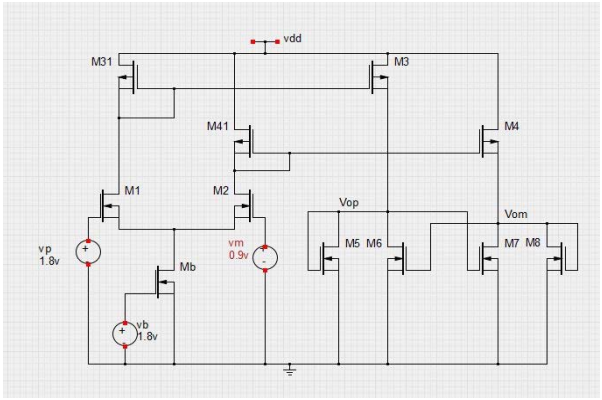

Fig-3: Decision making circuit

After the pre-amplification stage, the low voltage is present in the M3. It can be given as the input to the M7, it gets off and thereby the output voltage at **vom is low**. Similarly the high voltage which is present in the M4 and it can be given as the input to the M6, it gets on and thereby the output voltage at **vop is high.** The simulation result for the measurement of voltage at two output nodes is shown below.

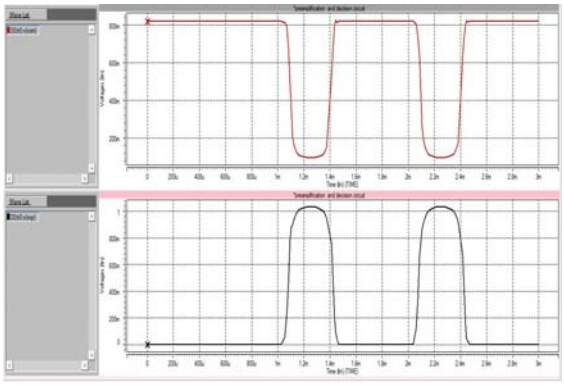

Fig-4: Simulation result

C. Post Amplification Circuit

This circuit also called as output buffer. It amplifies the signal and gives the output at logic levels. The schematic diagram and the corresponding waveforms are as shown below.

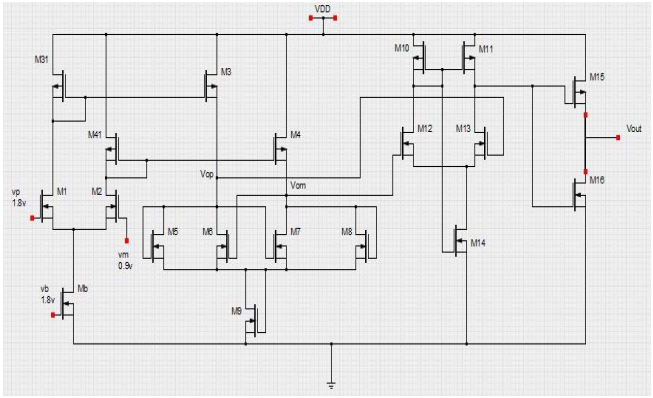

Fig -5: Post-Amplification

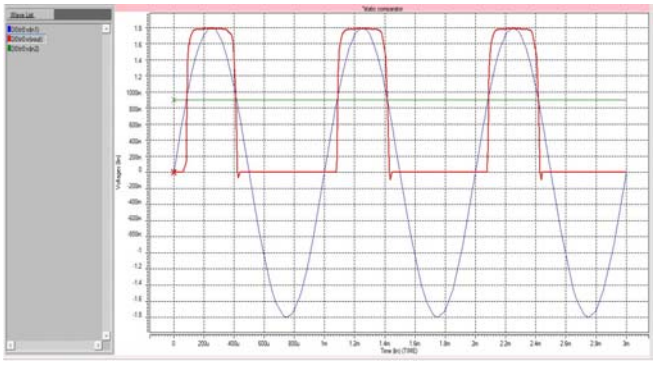

Fig -6: Simulation Result for static comparator

When vom is low and it makes the transistor M12 to be OFF. When vop is high and it is given as the input of M13, it gets ON and the output is pull down to ground. Now the inverter gets the input from the output node and gives the logic as 1(vdd).

II. SELECTION OF THE BIAS VOLTAGE

The bias voltage chosen based on the drain characteristics. By sweeping the values of the gate voltage for the maximum drain source voltage. Before finding the bias voltage, the total current is measured at the transistors M1 and M2. The total current is measured as 1.135mA. From the drain characteristics, the current is measured at the particular vgs curve and the gate voltage to be measured is 1.5v. The biasing circuit and their drain characteristics are as shown below.

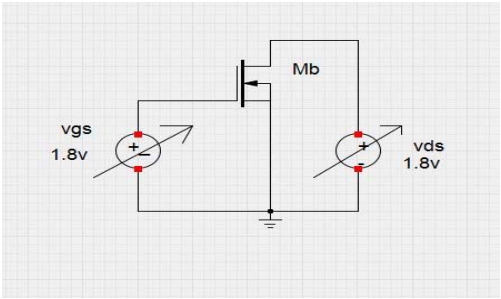

Fig -7: Biasing circuit

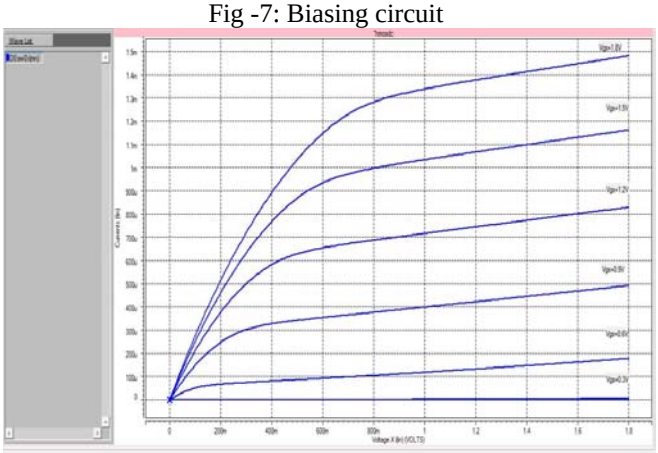

Fig -8: Drain characteristics

Therefore by using the proper biasing in the circuit, the under shoot and the overshoot problems avoided in the static comparator. The simulation result of the static comparator is as shown below.

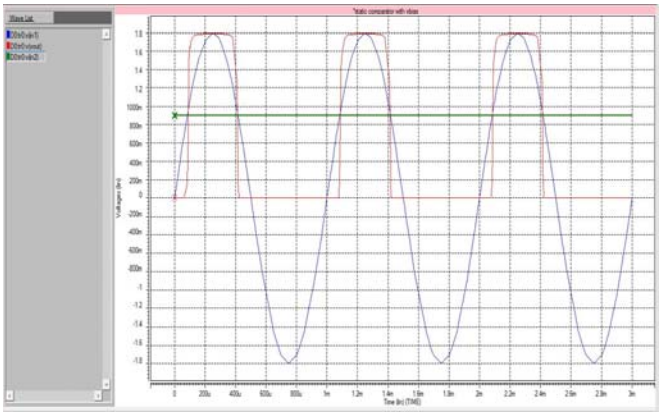

Fig -9: Simulation Result for static comparator with proper bias

III. WIDTH ADJUSTMENT OF MOS TRANSISTORS

The adjustment of the W/L ratio makes the changes in the rise time and fall time. The resistance of the PMOS is twice the resistance of the NMOS and so the mobility of the NMOS transistor is high. This affect the rise and fall time. In order to equalize the mobility of both the electrons and holes, the width of the NMOS and PMOS will be adjusted. That is the width of the PMOS is twice the width of the NMOS making the circuit having low rise time and fall time and it can be shown in the table.

TABLE -1
RISE AND FALL TIME CALCULATION

Comparator	Rise time(s)	Fall time(s)
Static comparator with same width(NMOS=PMOS=10/1)	17.11u	22.93u
Static comparator NMOS=10/1 PMOS=20/1	9.28u	15.68u

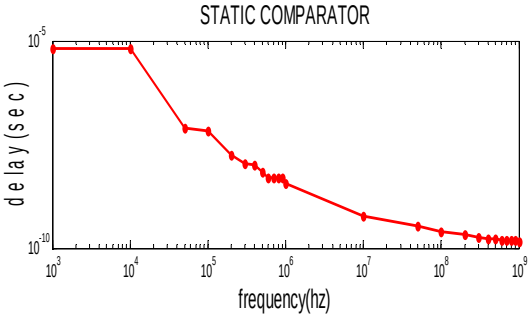

Fig -10: input frequency Vs delay

IV. STATIC LATCHED COMPARATOR

The first type of comparator called **static latched comparator** is represented in the fig. the operation of this comparator is as shown below.

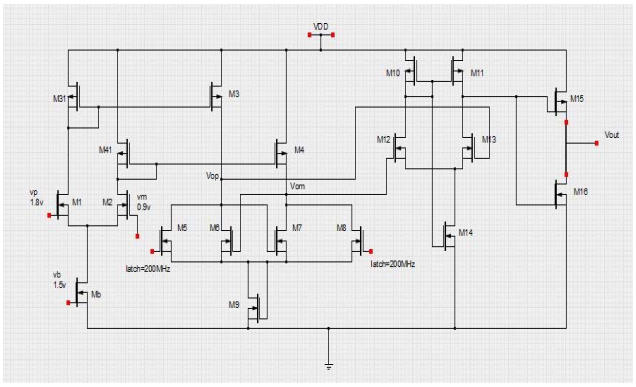

Fig -11: Static latched comparator

In the reset phase i.e. when latch is high the transistors M5/M8 turn ON and push the output to the ground. The transistors M1, M2, M31, and M41 behave as a pre-amplifier and the current is mirrored to the output nodes which are represented by vop and vom via M3 and M4. When the latch is low M5 and M8 turn OFF, the current flowing in M3/M4 charge the output nodes vop and vom. Based on the input voltages present in M1/M2 and the voltages at the output nodes makes the transistors M6/M7 either turn ON which starts the regeneration phase. The advantage of this comparator is that having low kickback noise. But some drawbacks affect the performance of this comparator (i) static power consumption (ii) slow regeneration process.

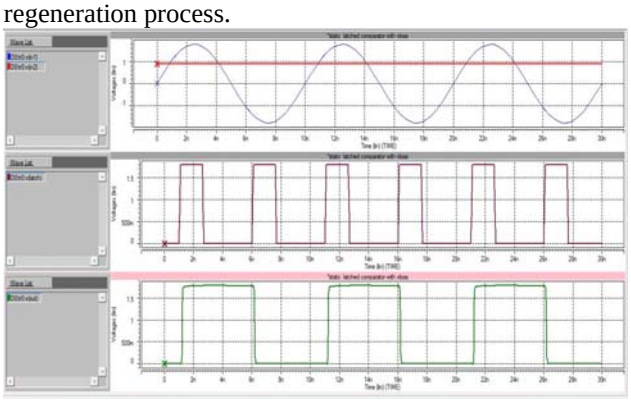

Fig -12: Simulation Result for static latched comparator

V. CLASS-AB LATCHED COMPARATOR

The class AB latched comparator avoids the speed limitation problems in static latched comparator as shown below.

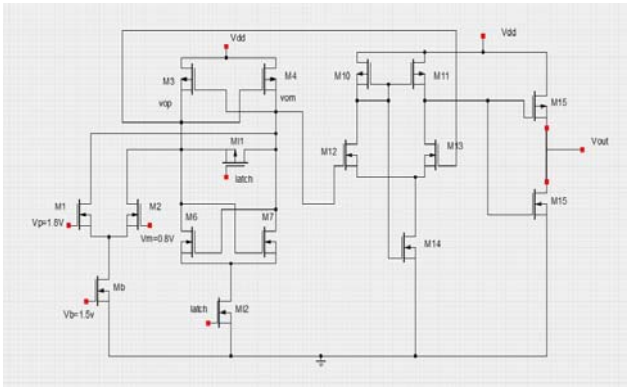

Fig -13: Class-AB latched comparator

In the reset phase, the latch is low, Ml2 get turned OFF and it prevents the current flowing in M6/M7. Ml1 acts as a reset switch and it provides the load to the differential pair represented by M1/M2. When the latch is high in regeneration phase, the reset switch turn ON and the transistor M4/M7 and M3/M6 form the two back to back inverters that regenerate the small output voltages in the initiation of this phase and converts into full scale digital levels. In this comparator, the speed is high due to the regeneration process and it can be done by the two cross coupled CMOS inverters. The drain terminal of the differential pair are directly connected to the regeneration nodes, therefore this circuit reacts faster according to the variation of the inputs. But these comparators having high speed and power efficient than the static comparator, but it generate more kickback noise. The simulation result is as shown below.

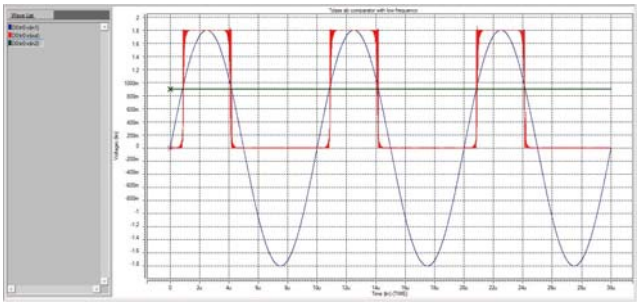

Fig -14: Simulation Result for Class-AB latched comparator

There are bunch of frequencies can be seen in this comparator output by using high frequencies. In order to avoid the bunch of frequencies we can put suitable capacitor in the output stage. If the capacitance value increased, the rise and fall time also increased. The effect of capacitance value and rise and fall time is as shown below.

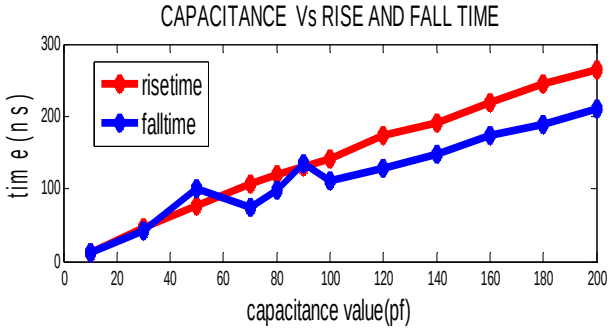

Fig -15: capacitance value Vs rise and fall time

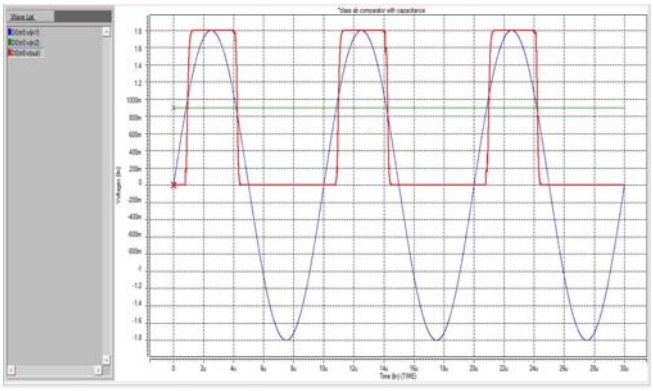

Fig -16: Simulation Result for Class-AB latched comparator with capacitor

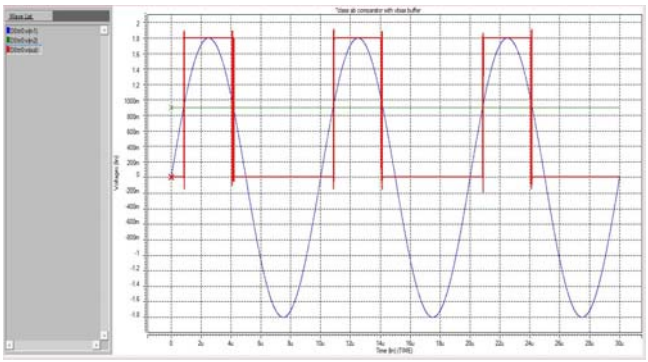

Fig -17: Simulation Result for Class-AB latched comparator with output buffer

When compared to all the method buffer method is the best one and it gives the fewer rises and fall time and thereby reduces the delay which in turn increases the speed of the comparator.

TABLE -2
RISE AND FALL TIME CALCULATION

Class AB latched Comparator	Rise time(s)	Fall time(s)
Low frequency (without capacitance)	910p	2.009n
With capacitance	142.16n	110.56n
With buffer	123p	228p

VI. DYNAMIC LATCHED COMPARATOR

Though the class AB latched comparators are more power efficient, but it have some supply current in the reset phase and after the regeneration phase completes. In the dynamic latched comparators, the current flow is only present in the regeneration phase. The schematic diagram is as shown below.

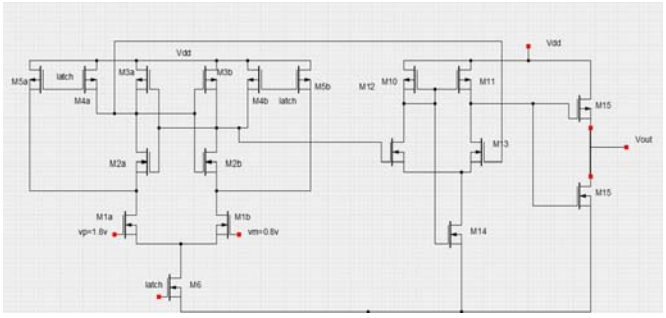

Fig -18: Dynamic latched comparator

In the reset phase when the latch is low, the transistors M4a/M4b and M5a/M5b turned ON and reset the output nodes, make the drains of the input differential pair connected to the VDD. The transistor M6 turns OFF and no current flows in it. In the regeneration phase, the latch goes high the transistors M4a/M4b and M5a/M5b turned ON the current flowing in M6 and in the transistors M1a/M1b. Based on the voltage given at the input, one of the cross coupled inverters produces the regeneration, M2a/M3a or M2b/M3b receives large current to find the output state. After the completion of the regeneration phase, one of the output nodes is at VDD and other output is at ground. The nodes present at the drains of the differential pair having rail-to-rail output and it causes the large kickback noise. There is another kickback noise present in this type of comparators. In the reset phase the current is not flow because M6 is in OFF condition. But in regeneration phase, the current flow in differential pair because M6 is ON and it has large V_{DS}. The voltages at the drains of the differential pair reaches zero it will move into the triode region. The triode region having changes due to the gate charges variation thereby causing the variation of the input voltages. This comparator is the fastest and power efficient but it has more kickback noise. The simulation result is as shown below.

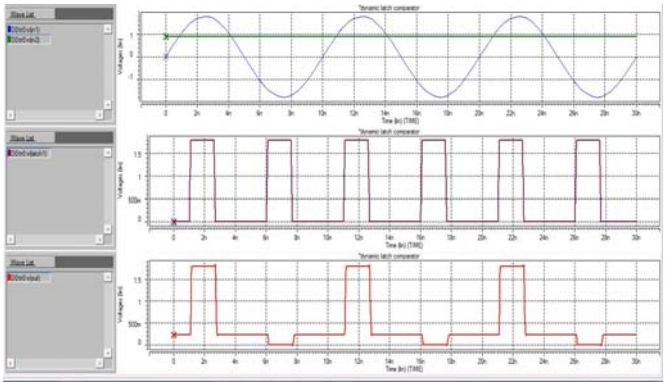

Fig -19: Simulation result of Dynamic latched comparator

VII. COMPARISON OF COMPARATORS

TABLE -3
RISE AND FALL TIME CALCULATION

Comparators	Rise time(s)	Fall time(s)
Static comparator	143.44p	310.58p
Static latched comparator	108.69p	36.64p
Class AB latched comparator	52.67p	298.44p
Dynamic latched comparator	36.47p	63.71p

The effect of latched frequency in the dynamic comparator and the static comparator is as shown below

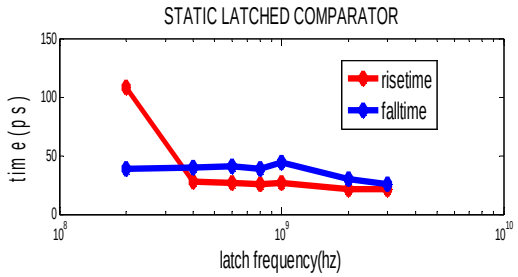

Fig -20: latch frequency Vs rise and fall time in static latched comparator

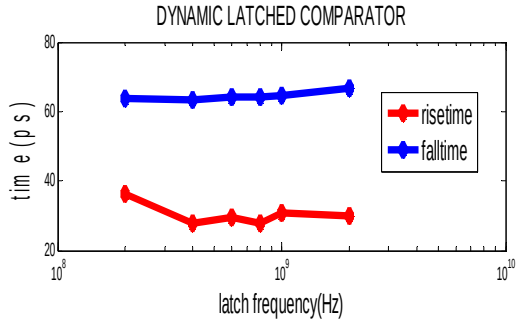

Fig -21: latch frequency Vs rise and fall time in dynamic latched comparator

The effect of supply voltage and the delay in the dynamic comparator and the static comparator is as shown below.

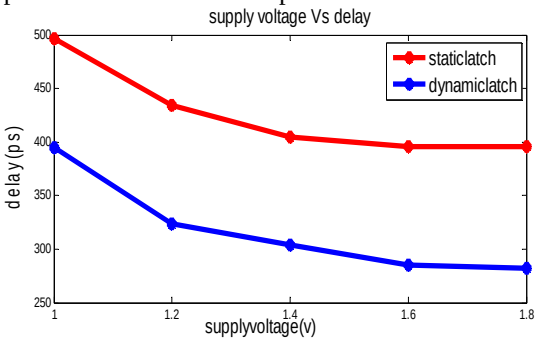

Fig -22: supply voltage Vs delay

VII. CONVENTIONAL DYNAMIC COMPARATOR

This comparator is widely used in analog to digital converters. The operation of the conventional dynamic comparator is explained below. The schematic diagram is as shown below.

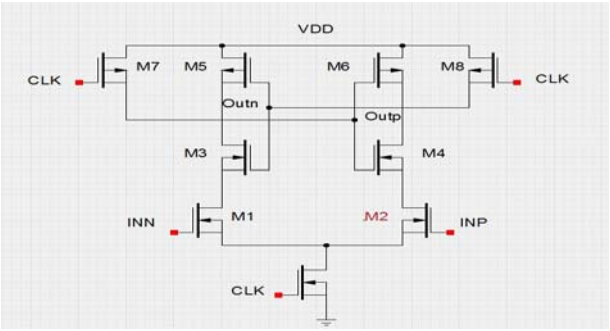

Fig -23: Conventional dynamic comparator

During the reset phase the CLK is LOW, Mtail is turned OFF. M7/M8 reset transistors pull the output node outn and outp to VDD to indicate the starting condition and provide the logical output. In the regeneration phase the CLK is HIGH, M7/M8 is turned OFF and Mtail is turned ON. The voltages present at the output nodes which have been already pre charged to VDD and it can start to discharge in different rates depend on the input voltages. If $V_{inp}>V_{inn}$ the outp discharges faster than the outn. Because outp discharged by the high drain current of M2. The node outn discharged by the low drain current of M1 transistor. The transistor M5 turned ON and starts the regeneration by connecting back to back inverters. Finally, the outn is at VDD and outp is at zero volt potential. This circuit works vice versa if $V_{inp}<V_{inn}$. The simulation result is as shown below.

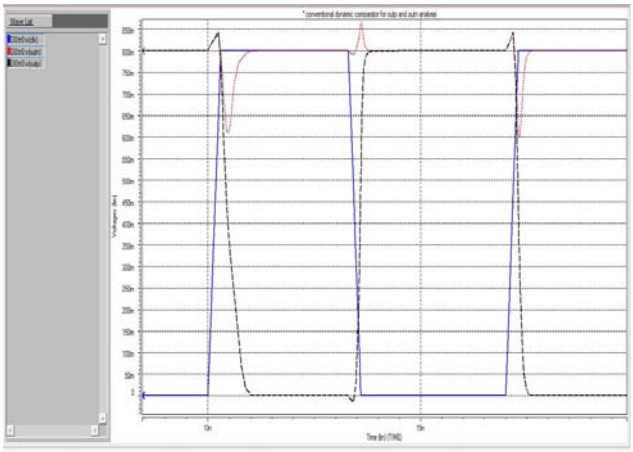

Fig -24: Simulation result of Conventional Dynamic Comparator

VIII. CONVENTIONAL DOUBLE- TAIL DYNAMIC COMPARATOR

In this comparator, less number of transistors is used and it can be operated at low supply voltage than conventional dynamic comparator. It has fast latching and low offset the schematic diagram is as shown below.

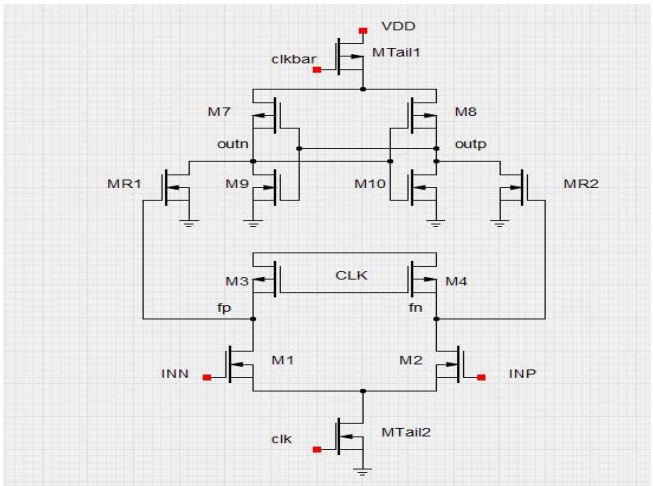

Fig -25: Conventional double tail dynamic comparator

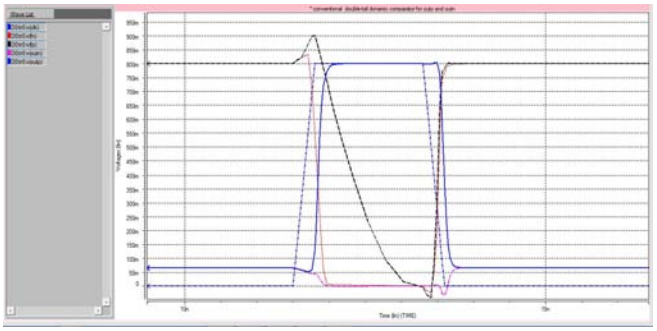

Fig -26: Simulation result of Conventional Double-Tail Dynamic Comparator

In reset phase CLK is low, MTail1 and MTail2 are turned OFF and thus M3/M4 turned ON, it can be pre charged the nodes fp and fn to VDD. This process causes the transistors MR1 and MR2 to discharge the fp and fn to ground. In regeneration phase CLK is high, MTail1 and MTail2 turned ON M3/M4 turned OFF and fp/fn starts to drop. The stages formed by the transistors MR1 and MR2 passes the voltages to the cross coupled inverters and provides the regeneration phase. This comparator has good insulation capability between the input and the output and thus the kickback noise is reduced. The simulation result is as shown below.

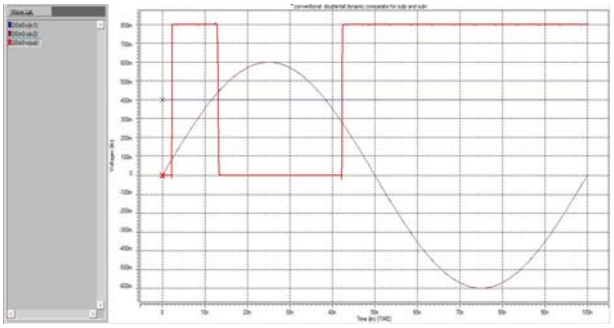

Fig -27: Simulation result of Conventional Double-Tail Dynamic Comparator

IX. PROPOSED DOUBLE- TAIL DYNAMIC COMPARATOR

The comparators with double tail structures give better performance in low power applications. Based on this a new double tail comparator is proposed. The schematic diagram is as shown below.

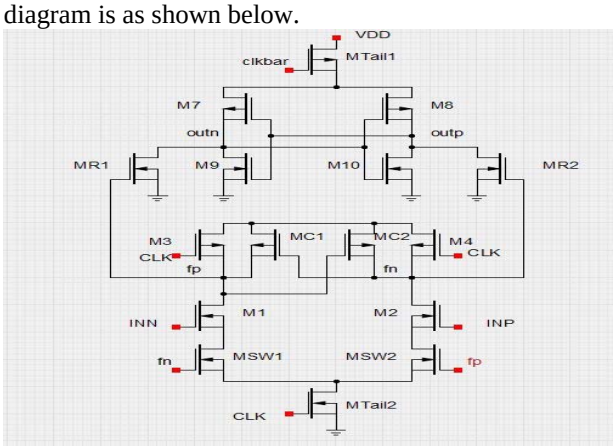

Fig -28: proposed double tail dynamic comparator

During the reset phase, the CLK is low, the transistors MTail1 and MTail2 turned OFF and this helps to reduce the static power consumption. The transistors M3/M4 turned ON which in turn makes the fp and fn nodes pull up to VDD. Then the control transistors MC1 and MC2 are turned OFF. The transistors present in the intermediate stage MR1 and MR2 pull the output nodes outp and outn to ground. In the regeneration phase when the CLK goes high, the transistors MTail1 and MTail2 gets turned ON. Now the nodes fp and fn discharge at different rates depend on the input voltages. The switching transistors SW1, SW2 are used to avoid the common mode voltage problem. SW1 and SW2 make the control transistors to increase their voltage difference. This comparator has low kickback noise, delay and low offset. If the clock frequency is increased then the speed of the comparator is also increases. The simulation result is as shown below.

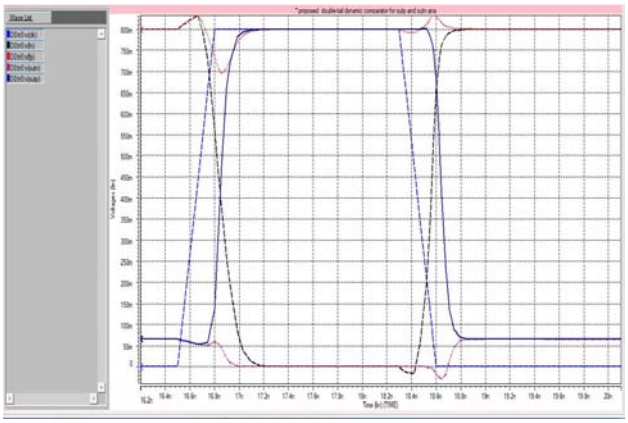

Fig -29: Simulation result of proposed Double-Tail Dynamic Comparator

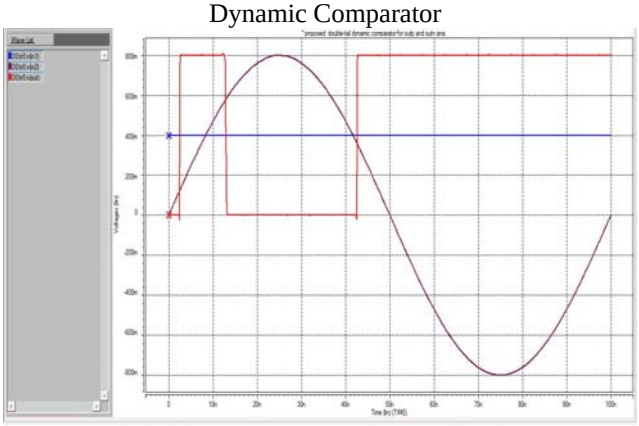

Fig -30: Simulation result of Proposed Double-Tail Dynamic Comparator

TABLE -3: SUPPLY VOLTAGE AND DELAY ANALYSIS

Dynamic Comparators	Supply voltage	Speed	Delay(ps/dec)
Conventional dynamic comparator	0.8V	900MHz	940
Conventional dynamic double tail comparator	0.8V	1.8GHz	358
Proposed dynamic double tail comparator	0.8V	2.4GHz	294

X. CONCLUSION

In this paper, different comparators have been analysed and why the dynamic comparator is chosen for high speed applications in ADCs circuits. When compared to all the existing comparators, the dynamic comparator having better performance. Among all the dynamic comparators the proposed double tail dynamic comparator having less delay and high speed. But if the speed is increased the kickback noise is also increased. In order to avoid the kickback noise, neutralization technique is used here. Our future work is to reduce the offset voltage by using body trimming method. The simulation results in 180nm CMOS technology shows that the delay and speed of the proposed comparator is reduced to a maximum extent in comparison with the conventional dynamic comparator and Double-tail comparator dynamic comparator.

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